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## NOTICE OF ALLOWANCE AND FEE(S) DUE

25570

7590

12/01/2008

ROBERTS MLOTKOWSKI SAFRAN & COLE, P.C.  
Intellectual Property Department  
P.O. Box 10064  
MCLEAN, VA 22102-8064

EXAMINER

WEST, JEFFREY R

ART UNIT

PAPER NUMBER

2857

DATE MAILED: 12/01/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,297	01/22/2002	Heinz Walter	740116-358	4774

TITLE OF INVENTION: ELECTRICAL TRANSDUCER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	03/02/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. **PROSECUTION ON THE MERITS IS CLOSED.** THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN **THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE** OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. **THIS STATUTORY PERIOD CANNOT BE EXTENDED.** SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

## HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER:** Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

# **PART B - FEE(S) TRANSMITTAL**

**Complete and send this form, together with applicable fee(s), to:** Mail **Mail Stop ISSUE FEE**  
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**P.O. Box 1450**  
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**INSTRUCTIONS:** This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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25570 7590 12/01/2008

**ROBERTS MLOTKOWSKI SAFRAN & COLE, P.C.**  
 Intellectual Property Department  
 P.O. Box 10064  
 MCLEAN, VA 22102-8064

## **Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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nonprovisional	NO	\$1510	\$300	\$0	\$1810	03/02/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
WEST, JEFFREY R	2857	702-057000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.  
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a **Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 \_\_\_\_\_  
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 \_\_\_\_\_  
 3 \_\_\_\_\_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee  
☐ Publication Fee (No small entity discount permitted)  
☐ Advance Order - # of Copies \_\_\_\_\_

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.  
☐ Payment by credit card. Form PTO-2038 is attached.  
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number \_\_\_\_\_ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature \_\_\_\_\_ Date \_\_\_\_\_  
 Typed or printed name \_\_\_\_\_ Registration No. \_\_\_\_\_

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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WEST, JEFFREY R

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ROBERTS MLOTKOWSKI SAFRAN & COLE, P.C.  
Intellectual Property Department  
P.O. Box 10064  
MCLEAN, VA 22102-8064

## Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 152 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 152 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

**Notice of Allowability****Application No.**

10/051,297

**Applicant(s)**

WALTER ET AL.

**Examiner**

Jeffrey R. West

**Art Unit**

2857

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the Appeal Brief filed 28 August 2008.
2. ☒ The allowed claim(s) is/are 1,4-17,20 and 21.
3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some\* c) ☐ None of the:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.  
(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached  
1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.  
(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.  
**Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08),  
Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_.

/Jeffrey R. West/  
Primary Examiner, Art Unit 2857

## **DETAILED ACTION**

### ***Drawings***

1. As noted in the Final Office Action mailed October 11, 2007, the informal drawings filed January 21, 2005, were accepted. Formal drawings must be filed in response to this Notice of Allowability.

## **EXAMINER'S AMENDMENT**

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

3. Authorization for this examiner's amendment was given in a telephone interview with David S. Safran (Reg. #27,997) on November 21, 2008.

The application has been amended as follows:

In claim 1, line 22, "comprises analog" has been changed to ---comprises an analog---.

In claim 6, line 1, "the analog" has been changed to ---the at least one analog--.

In claim 10, line 2, "of a single" has been changed to ---of the single---.

In claim 14, line 3, "to said one of the power" has been changed to ---to said one of the three power---.

In claim 16, line 20, "comprises analog" has been changed to ---comprises an analog---.

In claim 17, "wherein at least one active integrator, as an actuator for at least one direct current signal, is connected to the processor circuit and to the analog scaling unit" has been changed to ---wherein the at least one active integrator is an actuator for said at least one direct current signal---.

4. The following is an examiner's statement of reasons for allowance:

DE Patent No. 4016922 to Popp discloses an electrical transducer using a two-wire process (001) comprising an analog sensor that detects a quantity to be measured (009, lines 2-6), an analog end stage which is connected downstream of the sensor at the output end of the transducer (010, lines 32-35 and "13" in Figure 1), a processor circuit (010, lines 26-27 and "7" in Figure 1), wherein the processor circuit is not connected serially between the sensor and the analog end stage so that an analog measurement signal transmission path is realized (Figure 1), the analog end stage converting an output signal of the sensor into an impressed output current with a magnitude which is a measure of the quantity to be measured and is fixed within a range of about 0 to 20 mA, specifically about 4 to 20mA (010, lines 32-36 and Figure 1), the electrical transducer being controlled by the processor circuit (004, lines 1-8).

Popp discloses the analog measurement signal transmission path including an analog scaling unit ("6" in Figure 1), the output signal of the sensor and at least one analog setting value are supplied to the analog scaling unit (010, lines 1-8 and Figure 1), and the output signal of the analog scaling unit is supplied to the analog end stage (Figure 1).

Popp discloses that the analog scaling unit is an analog arithmetic circuit to which as the at least one analog setting value a DC voltage signal is delivered (010, lines 1-11) wherein the analog arithmetic circuit comprises at least one analog multiplier and at least one sign-evaluating (i.e. adding or subtracting) accumulator acting as an adder and/or subtractor (010, lines 11-19).

Popp discloses a power source that produces a non-zero output current (002, lines 14-16).

U.S. Patent No. 5,416,723 to Zyl teaches a loop powered process control transmitter operating at a loop power of between 4 and 20 mA (column 1, lines 5-16) wherein during normal operation of the process control transmitter, the microprocessor circuit is shifted temporarily from an awake mode into a sleep mode in which the processor circuit is inactive (column 2, lines 20-30 and column 3, lines 14-18).

U.S. Patent No. 5,886,565 to Yasui teaches a reference voltage generating circuit having an integrator that generates a reference voltage using a voltage

dividing circuit that divides a voltage supplied from a power source for use by the integrator (abstract).

U.S. Patent No. 5,714,903 to Bruccoleri et al. teaches a low-consumption analog multiplier that is a single-quadrant multiplier (column 4, line 66 to column 5, line 3).

U.S. Patent No. 3,805,092 to Henson teaches an electronic analog multiplier comprising a plurality of transistors (abstract) and a plurality of operational amplifiers (column 4, lines 32-38 and Figure 3).

U.S. Patent No. 6,057,794 to Takamuki teaches a sigma-delta modulation circuit as part of an analog-digital converter (column 1, lines 6-8) including an analog multiplier, adder, and subtractor (column 10, lines 5-14) with an adder connected through a delay circuit and a converter to the input of a multiplier and an adder and subtractor connected to the output of the multiplier (Figure 5).

U.S. Patent No. 5,207,101 to Haynes discloses a two-wire ultrasonic transmitter comprising a sensor that detects a quantity to be measured (column 2, lines 19-22), an analog end stage, comprising an amplifier circuit, connected downstream of the sensor (Figure 4b, "52"), a processor circuit, including a processor and drive circuit (column 7, lines 41-42) and an analog measurement signal transmission path (see subsequent circuitry from X1 in Figure 4a), the analog end stage including, between



the analog scaling unit and the subsequent analog end stage circuitry, an attenuator comprising an RC element (column 2, lines 58-60 and column 8, lines 52-64), having an adjustable time constant (i.e. adjustable resistor and capacitor values) wherein an error output of the attenuator can be compensate by a control circuit (i.e. comparator with threshold detection) (column 8, line 65 to column 9, line 9).

U.S. Patent No. 5,252,967 to Brennan et al. teaches a reader/programmer for two and three wire utility data communications system comprising a connector for connection to three or two power supply terminals (column 6, lines 18-25) wherein when a detector means determines that power is supplied to either the three or two power supply terminals, the device automatically switches between two and/or three wire operation modes (i.e. when the device detects a connection to the two-wire port or to the three wire port, the mode is automatically switched) (column 19, line 11 to column 20, line 5).

U.S. Patent No. 6,571,111 to Mayo et al. teaches a method and apparatus for reducing battery power consumption of transceivers in a communication network using an external generated timing signal wherein power consumption is reduced in each of the devices during a sleep period of a synchronized timing interval, the sleep period being significantly longer than the awake period.

U.S. Patent No. 6,388,617 to Flood et al. teaches a radio beacon with a GPS interface for automatically activated EPRIBs wherein a microprocessor is operated in an awake mode and a sleep mode wherein the sleep mode is more than 98% of the time.

U.S. Patent No. 4,524,624 to Di Noia et al. teaches a pressure and differential pressure detector and transmitter for use in hostile environments including a detector arrangement comprising an adder, subtractor, and multiplier.

U.S. Patent No. 5,956,663 to Eryurek teaches a signal processing technique which separates signal components in a sensor for sensor diagnostics.

U.S. Patent No. 5,083,091 to Frick et al. teaches a charge balanced feedback measurement circuit.

JP Patent Application Publication No. 04-359399 to Tamura et al. teaches a three-wire signal processor that converts a three-wire signal into a two-wire signal.

U.S. Patent No. 3,948,098 to Richardson et al. teaches a vortex flow meter transmitter that can be used in two-wire or three-wire operation.

As noted above, the cited prior art teaches many of the features of the claimed invention. Additionally, while the invention of Popp specifically discloses, in paragraph 004, that the dynamic sensing is carried out on the analog transmission path only and the processor is only for corrections, Popp is not explicit that the processor is inactive until the corrections are carried out by the processor. Without such explicit disclosure, it can be considered that the processor of Popp continuously, at a low clock frequency, and actively receives and processes data from the analog transmission path and only applies the corrections intermittently, thereby providing a processor that is always actively processing. Therefore, while Zyl teaches a loop powered process control transmitter operating at a loop power of between 4 and 20 mA wherein during normal operation of the process control transmitter, the microprocessor circuit is shifted temporarily from an awake mode into a sleep mode in which the processor circuit is inactive, the proposed combination would eliminate the continuous processing of Popp. Additionally, even if the proposed combination would properly shift the processor of Popp into sleep mode when the processor is inactive, the proposed combination falls short of explicitly providing a processor having an activity time, in which the processor circuit is active, which is shorter than the time that the processor circuit remains in the sleep mode, in which the processor circuit is inactive.

As such, with respect to claim 1, the cited prior art fails to sufficiently teach or suggest, in combination with the other claimed limitations for an electrical transducer using a two-wire process comprising an analog sensor that detects a quantity to be

measured; an analog end stage which is connected downstream of the sensor at the output end of the transducer; a processor circuit; and wherein the processor circuit is not connected serially between the sensor and the analog end stage so that a separate analog measurement signal transmission path is realized, the analog end stage converting an output signal of the sensor into an impressed output current with a magnitude which is a measure of the quantity to be measured and is fixed within a range of about 0 to 20 mA, the analog measurement signal transmission path including an analog scaling unit, the output signal of the sensor and at least one analog setting value are supplied to the analog scaling unit, and the output signal of the analog scaling unit is supplied to the analog end stage; wherein the processor circuit has an activity time in which the processor circuit is active which is shorter than the time that the processor circuit remains in the sleep mode in which the processor circuit is inactive; wherein the analog scaling unit comprises analog arithmetic circuit; wherein said at least one analog setting value is a DC voltage signal or a direct current signal which is delivered to the analog arithmetic circuit of the analog scaling unit; and wherein at least one active integrator is connected to the processor circuit and to the analog scaling unit as an actuator for producing said DC voltage signal or direct current signal.

Similarly, with respect to claim 16, the cited prior art fails to sufficiently teach or suggest, in combination with the other claimed limitations for a method of producing an indication of a measured value with an electrical transducer, the transducer comprising a sensor, an analog end stage which is connected downstream of the

sensor at the output end of the transducer, an electronic circuit which is connected downstream of the sensor, and a processor circuit which is not connected serially between the sensor and the analog end stage so that an analog measurement signal transmission path is realized, the electronic circuit converting an output signal of the sensor into an impressed output current with a level corresponding to the measured value and is fixed within a range of about 0 to 20 mA, the output signal of the sensor is supplied to an analog scaling unit, at least one analog setting value is supplied to the analog scaling unit, and the output signal of the analog scaling unit is supplied to the electronic circuit; wherein the processor circuit has an activity time in which the processor circuit is active which is shorter than the time that the processor circuit remains in the sleep mode, in which the processor circuit is inactive; wherein the analog scaling unit comprises analog arithmetic circuit; wherein said at least one analog setting value is a DC voltage signal or a direct current signal which is delivered to the analog arithmetic circuit of the analog scaling unit; and wherein at least one active integrator is connected to the processor circuit and to the analog scaling unit as an actuator for producing said DC voltage signal or direct current signal.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on (571)272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeffrey R. West/  
Primary Examiner, Art Unit 2857

November 27, 2008